(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 778 623 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
18.07.2001 Bulletin 2001/29

(51) Int Cl.7: **H01L 29/788**, H01L 27/115, G11C 16/04, H01L 21/82

(21) Application number: **96307350.7**

(22) Date of filing: **09.10.1996**

(54) PMOS memory cell with hot electron injection programming and tunnelling erasing

Durch heisse Elektroneninjektion programmierbare und durch Tunneleffekt löschbare PMOS-Speicherzelle

Cellule mémoire PMOS programmable par injection d'électrons chauds et effaçable par effet tunnel

(84) Designated Contracting States:
AT BE DE FI FR GB IT NL SE

(30) Priority: **14.11.1995 US 557589**

(43) Date of publication of application:
11.06.1997 Bulletin 1997/24

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EP-A- 0 079 636 **EP-A- 0 255 489**
EP-A- 0 618 621

- **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 35, no. 5, October 1992, NEW YORK US, pages 339-340, XP000312997 "High-speed, low-power/low-voltage P-channel NVRAM using channel-hot-carrier programming and tunneling erase through silicon-rich oxide"**

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Description

[0001] This invention relates to generally to non-volatile memory devices and specifically the very high density and high speed non-volatile devices.

[0002] Early semi-conductor memories employed P-channel floating-gate avalanche-injection MOS (FAMOS) devices. These devices are programmed by applying a 35 volt reverse bias across the N-well/drain junction such that high energy electrons generated by avalanche breakdown are injection from the depletion layer to the floating gate. The floating gate is typically erased, i.e., discharged, using UV radiation. In addition to having relatively slow operating speeds, the large reverse bias required for avalanche programming undesirably necessitates the on-chip generation of high voltages and also limits the extent to which the device size may be minimized.

[0003] As NMOS technology improved, manufacturers were able to take advantage of the faster intrinsic mobility of electrons, as compared with that of holes, and began fabricating N-channel memory devices such as EPROMs and EEPROMs which were faster and required lower programming voltages than FAMOS cells. A floating gate EPROM cell, such as the ETOX Flash EPROM cell manufactured by Intel Corporation of Santa Clara, CA, is charged by the hot injection of electrons from the N-channel/N+ drain junction region without an avalanche breakdown of the junction. Such programming may be realized for instance, by applying 12 volts to the control gate and 7 volts to the drain while grounding the source region. This electrical bias causes electrons to accelerate across the channel region toward the drain. The high energy electrons created near the N-channel/N+ drain junction by the resulting impact ionization are attracted by the more positive control gate voltage and are injected into the floating gate. Erasing is typically accomplished via electron tunneling by applying 12 volts to the source while grounding the control gate. Programming via hot carrier injection allows such an EPROM cell to be bit-programmable and therefore eliminates the need for a select transistor. However, charging the floating gate via hot electron injection from the N-channel/N+ drain region requires high programming currents and, therefore, results in high power consumption. Further, the ETOX Flash ERPOM cell described above suffers from read disturb and may have long term reliability problems as a result of high N+ source/P- substrate junction voltages during erasing. Moreover, erasing by bend to bend tunneling at the N+ source/P- substrate junction results in a high erase current, thereby consuming an undesirable amount of power during erasing.

[0004] The floating gate of a typical EEPROM memory cell is charged by the tunneling of electrons through a thin oxide layer insulating the floating gate from the source, drain, and channel. For instance, such an EEPROM cell may be erased by applying 20 volts to the control gate while the source, drain, and substrate are grounded. The resultant electric field causes electrons to tunnel through the oxide layer from the source, drain, and channel to the floating gate. Programming, i.e., discharging the floating gate, may be accomplished by holding the control gate at ground while applying 20 volts to the drain, thereby reversing the electric field and pulling electrons from the floating gate to the drain.

[0005] The EEPROM cell suffers from several drawbacks. First, in order to facilitate electron tunneling, a tunnel window must be opened in a region of the gate oxide primate to the drain. This tunnel opening not only increases the size of the storage cell but also increases fabrication complexity and cost. Second, each EEPROM cell requires its own select transistor in order to be bit addressable during programming and reading. Further, such EEPROM cells require relatively high programming and erasing voltages of approximately 20 volts. The application of such high programming and erasing voltages across P/N junction within the EEPROM cell undesirably limits the amount by which the cell size may be reduced.

[0006] In addition, high programming and erasing voltages can cause current to leak between adjacent memory cells, resulting in a decrease in read current and read speed. European Patent Application 0 618 621 to Hayakawa discloses a NAND type EEPROM array for increasing the read current and read speed. However, the device of Hayakawa still utilizes high programming and erasing voltages.

[0007] More recently, P-channel memory cells have been manufactured and used where programming and erasing of this cell occur in the enhancement mode, such as the P-channel NVRAM cell disclosed in IBM technical disclosure bulletin, Volume 35, number 5, of October 1992, pages 339 to 340 and the P-channel MOS device disclosed in EP patent publication 0 255 489. However, these types of memory cells are programmed in the enhancement mode, therefore the amount of programming control for the cell, in addition to the current available for read operations, are limited.

[0008] Methods of operating a semiconductor memory cell to programme said cell or to erase said cell are defined in claims 1-4 of the accompanying claims.

[0009] The invention will now be described by was of example only, with reference to the accompanying drawings, in which:

Figure 1 is a cross-sectional view of a memory cell as used in accordance with the present invention;
Figures 2A and 2B are cross-sectional views of a portion of the cell of Figure 1 illustrating programming of the cell;
Figure 2C is a cross-sectional view of a portion of the cell of Figure 1 illustrating erasing of the cell;
Figure 3 is an array employing the cells of Figure 1;

Figure 4 is a cross-sectional view of the cell of Figure 1 implemented as part of a NOR cell;
Figure 5 is an array employing the cells of Figure 4;
Figure 6 is a cross-sectional view of the cell of Figure 1 implemented as part of a Flash cell;
Figure 7 is an array employing the cells of Figure 6;
Figure 8 is a cross-sectional view of the cell of Figure 1 implemented as part of an EEPROM cell;
Figure 9 is an array employing the cells of Figure 8; and
Figures 10-13 illustrate the fabrication of a P-channel memory cell in accordance with the present invention.

[0010] Referring to Figure 1, a flash memory cell 10 has a channel 12 extending between P+ source 14 and P+ drain 16 regions formed in an N- well 18 of a P-substrate 20. Note that although shown in Figure 1 as being formed in N-well 18, cell 10 in other embodiments may be formed in any other suitable underlying N- type structure. A floating gate 22 is insulated from the surface of N- well 18 by a thin tunneling oxide layer 24. In the device shown in Figure 1, tunneling oxide layer 24 has a thickness of approximately 80-130 Å and extends over the entire length of channel 12 and portions of both P+ source 14 and P+ drain 16. It is to be understood, however, that in other embodiments tunneling oxide layer 24 may of other varying lengths, length being in the direction indicated by arrow 25. For instance, in one device (not shown), tunneling oxide layer 24 extends only over a portion of P+ drain 16, wherein the remaining surface of N- well 18 has a thick gate oxide layer formed thereon.

[0011] A control gate 26 is insulated from floating gate 22 by an insulating layer 28 having a thickness of approximately 180-350 Å. In this device, cell 10 should, in its normal or erased state, have a threshold voltage V_T equal to approximately -1.0 to -5.0 V depending upon the particular cell and the configuration of its associated array. The particular value of V_T may be altered by conventional ion implanting of dopants into channel region 12.

[0012] The operation of cell 10 is as follows. To program cell 10, approximately 8 V is applied to P+ source 14 and N- well 18 while drain 16 is held at 2V. The voltage at control gate 26 is ramped up from V_{cc} to approximately 12 V. Acceptable ranges for these programming voltages are listed below in Table 1. Now referring also to Figure 2A, positively charged holes near source 14 and channel 12 are attracted to the less positive voltage on P+ drain 16 and are accelerated through channel region 12 towards P+ drain 16, as indicated by arrow 1. These holes collide with electrons and lattice atoms in a drain depletion region 30, thereby resulting in image ionization, as indicated by star 2. The high energy electrons generated from impact ionization, attracted by the positive voltage on control gate 26, are injected from depletion region 30 into floating gate 22, as indicated by arrow 3. The resultant negative charge on floating gate 22 depletes channel region 12 and forces cell 10 into deep depletion. In the preferred embodiment, cell 10 has, in its programmed state, a V_T equal to approximately 4 V. The programming voltages mentioned above and listed in Table 1, by effecting such a low channel current PMOS hot electron injection (LCCPHEI) programming, allow cell 10 to be bit-selectable during programming.

[0013] In a preferred embodiment, cell 10 may be programmed by hot electron injection without a channel current. Referring now to Figures 1 and 2B, approximately 8 V is applied to an N-well 18, approximately 12 V is applied to control gate 26, and approximately 2 V is applied to P+ drain 16. P+ source 14 is at a floating potential. The reverse bias across the P+ drain 16 and N-well 18 junction, combined with the positive voltage coupled to floating gate 22 via control gate 26, creates a sufficiently high electric field in a region 31 near the interface of tunnel oxide layer 24 and depletion region 30 to generate high energy electrons which are injected from region 31 into floating gate 22, as indicated by arrow 3. In this manner, hot electron injection is induced by bend-to-bend tunneling.

[0014] To erase cell 10, approximately 17 volts is applied to P+ source 14, P+ drain 16, and N- well 18 while control gate 26 is grounded. Acceptable ranges for these erase voltages are listed below in Table 1 under "Erase Option 1". Referring also to Figure 2C, the equal bias voltages applied to P+ source 14, P+ drain 16, and N- well 18 attract electrons stored in floating gate 22 (Figure 2A). Electrons tunnel from floating gate 22 across the entire length of tunneling oxide layer 24 into channel 12, source 14, and drain 16, thereby returning the threshold voltage of cell 10 to that of its erased state. Note that electrons will tunnel from floating gate 22 and thereby erase cell 10 only if the drain 16 voltage is approximately 17 volts.

[0015] In another embodiment, cell 10 may be erased by applying approximately 8 volts to P+ source 14, P+ drain 16, and N- well 18 and applying approximately -8 volts to control gate 26. Acceptable ranges for such voltages are listed below in Table 1 as "Erase Option 2". The application of Option 2 erase voltages, which results in an erasing of cell 10 in manner identical to that described above with respect to Option 1, allows erasing voltages of only 8 volts to be used without any degradation in performance of cell 10. In this manner, cell 10 allows for High Endurance Selectable Channel (HESC) erasing.

[0016] Where it is desired to read cell 10, V_{cc} is applied as a read voltage to source 14 and N-well 18. A voltage between 0 and V_{cc}, depending upon the associated array configuration, is applied to control gate 26. A voltage less than V_{cc} is applied to P+ drain 16. Cell 10 will conduct a channel current only if cell 10 is programmed, i.e., only if charge is stored in floating gate 22. Thus, the voltage on floating gate 22 will be lower than the voltage on P+ source 14, P+ drain 16, and N-well 18. Further, when cell 10 is in an erased state, the voltage on floating gate 22 remains

lower than the voltage on P+ source 14, P+ drain 16, and N-well 18. As a result, cell 10 does not suffer from read disturb problems characteristic of conventional NMOS memory devices. Note that the voltage on floating gate 22 will be lower than the voltage on P+ source 14, P+ drain 16, and N-well 18 as long as the V_t of cell 10, with floating gate 22 uncharged, is less than or equal to approximately -4.5 V and the read voltages shown in Table 1 are utilized.

Table 1

	Drain	Control gate	Source	N-well
programming (with channel current)	0V to 2V	V_{cc} ramped up to 16V	floating	5V to 15V
programming (without channel current)	0V to 2V	5V to 16V	5V to 15V	5V to 15V
erase (option 1)	15V to 22V	0V	15V to 22V	15V to 22V
erase (option 2)	3V to 15V	(-15V) to (-3V)	3V to 15V	3V to 15V
Read	Less than VCC	0V to V_{cc}	VCC	V_{cc}

[0017] The above-described operation of cell 10 utilizes PMOS characteristics to achieve numerous other advantages over conventional semiconductor memory cells. The characteristic gate current for P-channel devices is approximately 100 times that of N-channel devices. Thus, unlike conventional NMOS memory cells which typically require approximately a 0.5 milli-amp programming current to charge the floating gate, cell 10 requires a programming current of only a few micro-Amps. Requiring a programming current two orders of magnitude smaller than that of conventional NMOS memory cells such as EPROMs not only allows cell 10 to reduce power consumption during programming but also allows for page writing, i.e., to simultaneously write to numerous ones of cells 10 in a row of an associated memory array (not shown).

[0018] It is known that the channel of conventional NMOS flash memory cells must be of a sufficient length to tolerate the typically high reverse bias voltage across the P-well/N+ drain junction (as well as the resultant high electric field) required during erasing via electron tunneling. As a result, it is difficult to further reduce the size of such conventional cells without incurring destructive junction stress which, in turn, may lead to reliability problems. Since, however, the operation of cell 10 neither requires nor utilizes such high junction biases during erasing (see Table 1), minimizing the channel length of cell 10 is not so limited. This feature allows cell 10 to be fabricated using technology, sub-micron technology, and in particular, technology producing feature sizes less equal to or less than 0.7 μm. Avoiding such high junction biases during erasing also advantageously results in a more durable and reliable memory cell.

[0019] Note that as the channel length of an NMOS transistor falls below approximately 0.7 μm, electron mobility saturates. In PMOS devices, however, hole mobility continues to increase as the channel length decreases below 0.7 μm and becomes comparable to electron mobility as the gate length is further decreased. Accordingly, minimizing the channel length of cell 10 also advantageously results in a hole mobility comparable to that of electrons, thereby increasing the speed of cell 10. Further, note that when programmed, cell 10 is in deep depletion. This allows for a higher read current and thus for faster read speeds.

[0020] Cell 10 may be employing in an array configuration a portion of which is shown in Figure 3. The sources 14 of cells 10a-10d are coupled to a common source node CS. The control gate 26 of cells 10 in a row are coupled to a word line for that row, and the drains 16 of cells 10 in a column are coupled to a bit line BL for that column. The bias conditions for programming and reading for instance cell 10a (and for erasing all of cells 10) are provided below in Tables 2A-2D.

Table 2A

Cell 10A voltages				
	Drain	Source	Control Gate	N-well
Program	0	Floating	4-10V	3.5-7V
Erase	3-15V	3-15V	-3 to -15V	3-15V
Read	less than V_{cc}	V_{cc}	0	V_{cc}

Table 2B

Cell 10B voltages				
	Drain	Source	Control Gate	N-well
Program	Floating	Floating	4-10V	3.5-7V
Erase	3-15V	3-15V	-3 to -15V	3-15V
Read	Floating	V_{cc}	0	V_{cc}

Table 2C

Cell 10C voltages				
	Drain	Source	Control Gate	N-well
Program	Floating	Floating	0	3.5-7V
Erase	3-15V	3-15V	-3 to -15V	3-15V
Read	less than V_{cc}	V_{cc}	V_{cc}	V_{cc}

Table 2D

Cell 10D voltages				
	Drain	Source	Control Gate	N-well
Program	0	Floating	0	3.5-7V
Erase	3-15V	3-15V	-3 to -15V	3-15V
Read	Floating	V_{cc}	V_{cc}	V_{cc}

[0021] The above described cell 10 may be employed as part of a larger NOR memory array. Figure 4 shows a 2-transistor memory cell 30 including a P-channel MOS transistor 32 as the bit line select transistor 32 and cell 10 as the storage transistor. Select transistor 32 includes a P+ source 16 (note that P+ region 16 also serves as drain 16 for cell 10) and a P+ drain 34 formed in N-well 18. Current flow through select transistor 32 is controlled by a gate 36. A bit line BL is coupled to drain 34 of select transistor 32.

[0022] The electric bias conditions for programming, erasing, and reading cell 30 are summarized below in Table 3. Since cell 30 includes P-channel cell 10 and P-channel select transistor 32, cell 30 realizes all the advantages discussed above with respect to cell 10. When provided as part of a NOR memory array, cell 10, when programmed, operates as a depletion device.

Table 3

	Bit line	select gate	control gate	Source	N-well
programming (with channel-current)	0V	0V	vcc ramp up to 16V	5 V to 15V range	5V to 15V range
programming (without channel current)	0V	0V	5V to 16V range	5V to 15V range	5V to 15V range
erase (option 1)	15V to 22V range	0V	0V	15V to 22V range	15v to 22V range
erase (option 2)	3V to 15V range	0V	(-15V) to (-3V) range	3V to 15V range	3V to 15V range
Read	Less than Vcc	0V	0 to Vcc	Vcc	Vcc

[0023] Figure 5 shows a portion of a NOR array 40 employing as memory elements cell 30. The sources 14 of each

of cells 10 in array 40 are coupled to a common source node CS. In one embodiment P+ sources 14 of cells 10 may be shorted to N-well 18 by N+ pick-up implants (not shown). The drain 34 of each bit line select transistor 32 in a column are coupled to a bit line BL for that column. The control gates 26 of cells 10 in a row are coupled to a control gate line CG for that row, while the gates of bit line select transistors 32 in a row are coupled to a word line WL for that row.

[0024] Array 40 is bit programmable using low voltages and low current, and may be erased in bulk using low voltages and low current. Note that the control gates 26 of cells 10 may be held at the same potential and thus do not need to be decoded, i.e., the selected and unselected control gates may be held at the same potential. This allows for a simpler design. The preferred bias conditions and acceptable ranges for bias conditions operating NOR array 40 employing cells 30 in accordance with the present invention are listed below in Tables 4A and 4B, respectively, where NOR array 40 is operating on a supply voltage (not shown) V_{cc}.

Table 4A

	Bit Line		Word Line		Cell Gate CG	C'mon Source	N-well
	selected	unselected	selected	unselected			
read	V_{cc} - 2V	Floating	0	V_{cc}	V_{cc}-2V	V_{cc}	V_{cc}
erase	8V	n/a	0	n/a	-8V	8V	8V
program	0	8V or floating	0	8V	0V ramped to 12V	8V	8V

Table 4B

	Bit Line		Word Line		Cell Gate CG	C'mon Source	N-well
	selected	unselected	selected	unselected			
read	less than V_{cc}	Floating	0-2V	V_{cc}	less than V_{cc}	V_{cc}	V_{cc}
erase	3-15V	n/a	0	n/a	-3 to -15V	3-15V	3-15V
program	0	5-15V	0	5-15V	0V ramped to 12V	5-15V	5-15V

[0025] The above described embodiments may also be employed as part of a larger flash memory array. Figure 6 shows a 2-transistor memory cell 50 including a P-channel MOS transistor 52 as the source select transistor and cell 10 as the storage transistor. Select transistor 52 includes a P+ source 54 formed in N-well 18 and a gate 56. Source 14 of cell 10 serves as a drain for select transistor 52. A bit line BL is coupled to drain 16 of storage cell 10. Since cell 50 includes P-channel cell 10 and P-channel source select transistor 52, cell 50 realizes all the advantages discussed above with respect to cell 10.

[0026] Figure 7 shows a portion of a Flash array 60 employing as memory elements cell 50. The source 54 of each of source select transistor 52 of cells 10 in array 60 is coupled to a common source node CS. In one embodiment P+ sources 14 of cells 10 may be shorted to N-well 18 by N+ pick-up implants (not shown). The drain 16 of each of cells 10 in a column is coupled to a bit line BL for that column. The gates 56 of source select transistors 52 in a row are coupled to a first word line WL1 for that row. The control gates 26 of cells 10 in a row are coupled to a second word line WL2.

[0027] Array 60 is bit programmable and may be erased in either bulk or sector modes. In the operation of array 60, both the first word line WL1 and the second word line WL2 voltages need to be decoded. Note that provided as part of a flash memory array, cell 10, when programmed, operates as a depletion device.

[0028] The preferred bias conditions and acceptable ranges for bias conditions for operating array 60 employing cells 50 in accordance with the present invention are listed below in Tables 5A and 5B, respectively, where array 60 is operating on a supply voltage (not shown) V_{cc}.

Table 5A

	Bit Line		Word Line 1		Word Line 2		CS	N-well
	select	unselect	select	unselect	select	unselect		
read	V_{cc}-1.5V	Float	V_{cc}-2V	V_{cc}-2V	0	V_{cc}	V_{cc}	V_{cc}
sector erase	8V	0	8V	8V	-8V	-8V	8V	8V

Table 5A (continued)

	Bit Line		Word Line 1		Word Line 2		CS	N-well
	select	unselect	select	unselect	select	unselect		
bulk erase	8V	0	0	0	-8V	-8V	8V	8V
p'gram	0	6V	0	6V	ramp from 0 to 10V	0	6V	6V

Table 5B

	Bit Line		Word Line 1		Word Line 2		CS	N-well
	select	unselect	select	unselect	select	unselect		
read	less than V_{cc}	Float	less than V_{cc}	less than V_{cc}	0	V_{cc}	V_{cc}	V_{cc}
sector erase	3-15V	0	3-15V	3-15V	-3 to -15V	-3 to -15V	3-15V	3-15V
bulk erase	3-15V	0	0	0	-3 to -15V	-3 to -15V	3-15V	3-15V
p'gram	0	4-12V	0	4-12V	ramp from 0 to 10V	0	4-12V	4-12V

[0029] The above described embodiments may also be employed as part of a larger flash EEPROM memory array. Referring now to Figure 8, a 3-transistor memory cell 70 including storage cell 10 and both P-channel bit line select transistor 32 and P-channel source select transistor 52 which, as discussed earlier are connected to the drain and source, respectively, of cell 10. The drain 34 of bit line select transistor 52 is connected to bit line BL. Cell 70 realizes all the advantages discussed above with respect to cell 10.

[0030] Figure 9 shows a portion of an array 80 employing as memory elements EEPROM cells 70. The source 54 of each of source select transistor 52 of cells 10 in array 80 is coupled to a common source node CS. The drain of each of bit line select transistors 32 in a column is coupled to a bit line BL for that column. The gates 36 of bit line select transistors 32 in a row are coupled to a first word line WL1 for that row. The control gates 26 of cells 10 in a row are coupled to a control gate line CG. The gates 56 of each of source select transistors 52 in a row are coupled to a second word line WL2 for that row.

[0031] Array 80 is bit programmable and erasable in either bulk, sector, or bit modes and may be operated using low programming voltages and currents. Each of word lines WL1 and WL2 and control gate line CG may be advantageously held at the same potential and thus do not need to be decorded. Note that cell 10, when programmed, operates as a depletion device.

[0032] The preferred and acceptable ranges for bias conditions for operating array 80 employing cells 70 in accordance with the present invention are listed below in Tables 6A and 6B, where array 80 is operating on a supply voltage (not shown) V_{cc}.

Table 6A

	Bit Line		Word Line 1		Word Line 2		CG	CS	N-well
	select	unselect	select	unselect	select	unselect			
read	V_{cc}-2V	Float	0	V_{cc}	0	0 to V_{cc}	V_{cc}-2V	V_{cc}	V_{cc}
erase	8V	0	0	8V	8V	0	-8V	0	8V
p'gram	0	8V	0	8V	0	0 or 8V	ramp 0 to 12V	8V	8V

Table 6B

	Bit Line		Word Line 1		Word Line 2		CG	CS	N-well
	select	unselect	select	unselect	select	unselect			
read	less than V_{cc}	Float	0	V_{cc}	0	less than V_{cc}	less than V_{cc}	V_{cc}	V_{cc}
erase	3-15V	0	0	3-15V	3-15V	0	-3 to -15V	0	3-15V
p'gram	0	5-15V	0	5-15V	0	0 or 5-15V	ramp 0V to 12V	5-15V	5-15V

[0033] The fabrication of a cell 10 in accordance with the present invention will be discussed below in the context of a larger memory structure 100 which includes, in addition to a plurality of cells 10, a peripheral circuit having NMOS and PMOS transistors. Although the fabrication of cell 10 is described below as a twin-well process, cell 10 may also be fabricated according to an N-well process without departing from the scope of the present invention.

[0034] Referring now to Figure 10, structure 100 includes a P-type substrate 102 having formed by conventional means therein an N- well 104 and a P- well 106. The resistivity and thickness of N- well 104 and P- well 106 will depend upon the desired characteristics of the devices to be formed therein. Field oxide regions 108 approximately 7500 Å thick and a layer of pad oxide 110 approximately 240 Å thick are formed on a top surface of substrate 102 by any suitable means. A masking layer 112, which may be photo-resist or any other suitable masking material, is formed and then selectively etched using conventional methods to form the pattern shown in Figure 10.

[0035] N-type dopants such as Arsenic is implanted at an energy of approximately 100 keV (or Phosphorus at 50 keV) and a dosage of approximately 2E13 ions/cm^2 into a portion 111 of N-well 104 which will become in later steps channel 111 of cell 10. Masking layer 112 is then removed by a suitable etchant. After forming a tunnel oxide layer 114 approximately 80-130 Å thick, a poly-silicon layer is deposited over structure 100 and selectively etched to form floating gate 116. An ONO insulating layer 118 is formed and then selectively etched, as indicated in Figure 11, so as to completely overlie floating gate 116.

[0036] Portions of pad oxide 110 are removed using suitable etching techniques and a double layer of gate oxide 120 approximately having thicknesses of 120 Å and 250 Å, respectively, grown therein. A second poly-silicon layer is deposited and selectively etched to form control gate 122 of cell 10, gates 124 and 126 of PMOS peripheral transistors 10a and 10b, respectively, and gate 128 of NMOS peripheral circuit 10c. Note that PMOS peripheral transistors 10a and 10b and NMOS peripheral transistor 10c are representative of PMOS and NMOS peripheral circuitry, respectively, of cell 10's associated memory array (not shown).

[0037] Referring now to Figure 12, PMOS cell 10 and PMOS transistors 10a and 10b are masked. N-type dopants such as Phosphorus is implanted at an energy of approximately 40 keV and a dosage of approximately 3E13 ions/cm^2 into P-well 106 to form N- regions 130 and 132 which will serve as source and drain regions, respectively, of NMOS peripheral transistor 10c. This mask is removed. NMOS transistor 10c is then masked and P-type dopants such as BF_2 are implanted at an energy of approximately 60 keV and a dosage of approximately 7E12 ions/cm^2 into N-well 104 to form P-regions 134, 136, 138, and 140. Sidewall oxide spacers 142 are then formed by conventional means on the sides of control gate 122 and gates 124, 126, and 128.

[0038] PMOS cell 10 and PMOS transistors 10a and 10b are again masked and N-type dopants, which are preferably Arsenic, are implanted at an energy of 80 keV and a dosage of 5E15 ions/cm^2 into P-well 106 to form N+ diffusion regions 130a and 132a, as shown in Figure 13. The PMOS mask is then removed. Structure 100 is again masked and the sidewall spacers 142 on either side of control gate 122 are dipped. This ensures that in a subsequent doping step the source and drain regions of cell 10 will be of a P+ diffusion structure, as opposed to the lightly doped drain (LDD) structure of P-/P+ diffusion region 134/134a. After this mask is removed, NMOS transistor 10c is masked and P-type implants, preferably BF_2, are implanted at an energy of 50 keV and a dosage of 2E15 ions/cm^2 into N-well 104 to form P+ regions 134a, 136a, 138a, and 140a. Thus, P+ diffusion regions 136a and 138a serves as the source and drain regions, respectively, of cell 10. The N-/N+ diffusion regions 130/130a and 132/132a will serve as the source and drain regions, respectively, of NMOS transistor 10c, P-/P+ diffusion regions 134/134a and 136/136a will serve as the source and drain regions, respectively, of PMOS peripheral transistor 10a, and P-/P+ diffusion regions 138/138a and 140/140a will serve as the source and drain regions, respectively, of PMOS peripheral transistor 10b. The remaining portions of structure 100 may be completed according to well known fabrication techniques.

[0039] The process described above with respect to Figures 10-13 requires fewer masking steps than do conventional processes used in the fabrication of N-channel memory cells. The source and drain regions of cell 10 may be of the same dopant concentration and depth as the source and drain regions of PMOS peripheral transistors 10a and 10b.

Accordingly, a single masking-etching-doping sequence may be used to form the P+ source and P+ drain regions of cell 10 and the P+ source and P+ drain regions of PMOS peripheral transistors 10a and 10b, as described above. The fabrication of an N-channel memory cell requires an additional masking step since the source and drain regions of a conventional N-channel flash cell must be of a different dopant concentration than the source and drain regions of the NMOS peripheral transistors associated therewith. Note that the above-described process may also be used to form cell 10 and associated peripheral transistors 10a to 10c in an N-well structure.

Claims

1. A method of operating a semiconductor memory cell having an N-type well region (18) having formed therein a P+ source (14), a P+ drain (16), and a channel region (12) extending between said source and said drain; a first insulating layer (24) overlying said well region; a floating gate (22) overlying said first insulating layer; a second insulating layer (28) overlying said floating gate; and a control gate (26) overlying said second insulating layer, said method comprising:

   programming said cell by applying between approximately 5-15 volts to said P+ source (14) and to said N-type well region (18), applying approximately 0 to 2 volts to said P+ drain (16), and applying a voltage which ramps from a supply voltage to as high as approximately 16 volts to said control gate (26).

2. A method of operating a semiconductor memory cell having an N-type well region (18) having formed therein a P+ source (14), a P+ drain (16), and a channel region (12) extending between said source and said drain; a first insulating layer (24) overlying said well region; a floating gate (22) overlying said first insulating layer; a second insulating layer (28) overlying said floating gate; and a control gate (26) overlying said second insulating layer, said method comprising:

   programming said cell by applying between approximately 5-15 volts to said N-type well region (18), coupling said P+ source (14) to a floating potential, applying approximately 0 to 2 volts to said P+ drain (16), and applying between approximately 5-16 volts to said control gate (26).

3. A method of operating a semiconductor memory cell having an N-type well region (18) having formed therein a P+ source (14), a P+ drain (16), and a channel region (12) extending between said source and said drain; a first insulating layer (24) overlying said well region; a floating gate (22) overlying said first insulating layer; a second insulating layer (28) overlying said floating gate; and a control gate (26) overlying said second insulating layer, said method comprising:

   erasing said cell by applying between approximately 15-22 volts to said P+ source (14), to said N-type well region (18), and to said P+ drain (16) and grounding said control gate (26).

4. A method of operating a semiconductor memory cell having an N-type well region (18) having formed therein a P+ source (14), a P+ drain (16), and a channel region (12) extending between said source and said drain; a first insulating layer (24) overlying said well region; a floating gate (22) overlying said first insulating layer; a second insulating layer (28) overlying said floating gate; and a control gate (26) overlying said second insulating layer, said method comprising:

   erasing said cell by applying between approximately 3-15 volts to said P+ source (14), to said N-type well region (18), and to said P+ drain (16), and applying between approximately -3 to -15 volts to said control gate (26).

5. The method of Claim 1, wherein said cell further comprises a select transistor (32) formed in said N-type well region (18), said select transistor comprising a select gate (36) coupled to a word line, a P+ source coupled to said P+ drain (16) of said cell, and a P+ drain (34) coupled to a bit line, and a channel region extending between said P+ source and said P+ drain of said select transistor, wherein said cell operates on a supply voltage, and wherein said cell is programmed by applying between approximately 5-15 volts to said P+ source (14) and to said N-type well region (18), grounding said word line and said bit line, and applying a voltage which ramps from 0 to approximately 10 volts to said control gate (26).

6. The method of Claim 4, wherein said cell further comprises a select transistor (32) formed in said N-type well region (18), said select transistor comprising a select gate (36) coupled to a word line, a P+ source coupled to said P+ drain (16) of said cell, and a P+ drain (34) coupled to a bit line, and a channel region extending between said P+ source and said P+ drain of said select transistor, wherein said cell operates on a supply voltage, and wherein said cell is erased by applying between approximately 3-13 volts to said P+ source (14), to said N-type well region (18), and to said bit line, grounding said word line, and applying approximately - 3 to -15 volts to said control gate

(26).

7. The methods of Claim 1, wherein said cell further comprises a bit line select transistor (32) having a P+ source coupled to said P+ drain (16) of said cell, a P+ drain (34) coupled to a bit line, and a select gate (32) coupled to a first word line; and a source select transistor (52) having a P+ source (54), a P+ drain coupled to said P+ source (14) of said cell, and a gate (56) coupled to a second word line, wherein said structure operates on a supply voltage, and wherein said cell is programmed by applying between approximately 5 to 15 volts to said P+ source (54) of the source select transistor and to said N-type well region (18), grounding said first and second word lines and said bit line, and applying a voltage which ramps from 0 to as high as approximately 16 volts to said control gate (26).

8. The methods of Claim 4, wherein said cell further comprises a bit line select transistor (32) having a P+ source coupled to said P+ drain (16) of said cell, a P+ drain (34) coupled to a bit line, and a select gate (32) coupled to a first word line; and a source select transistor (52) having a P+ source (54), a P+ drain coupled to said P+ source (14) of said cell, and a gate (56) coupled to a second word line, wherein said structure operates on a supply voltage, and wherein said cell is erased by applying between approximately 3-15 volts to said N-type well region (18), to said second word line, and to said bit line, grounding said fist word line and said P+ source (54) of the source select transistor, and applying approximately -3 to -15 volts to said control gate (26).

Patentansprüche

1. Verfahren zum Betreiben einer Halbleiterspeicherzelle, die einen n-leitenden Quellbereich (18), in dem eine P+ Source (14), ein P+ Drain (16) und ein sich zwischen der Source und dem Drain erstreckender Channelbereich (12) ausgebildet ist, eine erste isolierende Schicht (24) über dem Quellbereich, ein potentialfreies Gate (22) über der ersten isolierenden Schicht, eine zweite isolierende Schicht (28) über dem potentialfreien Gate und ein Kontrollgate (26) über der zweiten isolierenden Schicht umfaßt, wobei das Verfahren
das Programmieren der Zelle durch Anlegen von ungefähr 5 bis 15 Volt an die P+ Source (14) und den n-leitenden Quellbereich (18), Anlegen von ungefähr 0 bis 2 Volt an den P+ Drain (16) und Anlegen einer von einer Versorgungsspannung bis auf ungefähr 16 Volt ansteigenden Spannung an das Kontrollgate (26) umfaßt.

2. Verfahren zum Betreiben einer Halbleiterspeicherzelle, die einen n-leitenden Quellbereich (18), in dem eine P+ Source (14), ein P+ Drain (16) und ein sich zwischen der Source und dem Drain erstreckender Channelbereich (12) ausgebildet ist, eine erste isolierende Schicht (24) über dem Quellbereich, ein potentialfreies Gate (22) über der ersten isolierenden Schicht, eine zweite isolierende Schicht (28) über dem potentialfreien Gate und ein Kontrollgate (26) über der zweiten isolierenden Schicht umfaßt, wobei das Verfahren
das Programmieren der Zelle durch Anlegen von ungefähr 5 bis 15 Volt an den n-leitenden Quellbereich (18), Anschließen der P+ Source (14) an ein potentialfreies Potential, Anlegen von ungefähr 0 bis 2 Volt an den P+ Drain (16) und Anlegen von ungefähr 5 bis 16 Volt an das Kontrollgate (26) umfaßt.

3. Verfahren zum Betreiben einer Halbleiterspeicherzelle, die einen n-leitenden Quellbereich (18), in dem eine P+ Source (14), ein P+ Drain (16) und ein sich zwischen der Source und dem Drain erstreckender Channelbereich (12) ausgebildet ist, eine erste isolierende Schicht (24) über dem Quellbereich, ein potentialfreies Gate (22) über der ersten isolierenden Schicht, eine zweite isolierende Schicht (28) über dem potentialfreien Gate und ein Kontrollgate (26) über der zweiten isolierenden Schicht umfaßt, wobei das Verfahren
das Löschen der Zelle durch Anlegen von ungefähr 15 bis 22 Volt an die P+ Source (14), den n-leitenden Quellbereich (18) und den P+ Drain (16) und Erden des Kontrollgates (26) umfaßt.

4. Verfahren zum Betreiben einer Halbleiterspeicherzelle, die einen n-leitenden Quellbereich (18), in dem eine P+ Source (14), ein P+ Drain (16) und ein sich zwischen der Source und dem Drain erstreckender Channelbereich (12) ausgebildet ist, eine erste isolierende Schicht (24) über dem Quellbereich, ein potentialfreies Gate (22) über der ersten isolierenden Schicht, eine zweite isolierende Schicht (28) über dem potentialfreien Gate und ein Kontrollgate (26) über der zweiten isolierenden Schicht umfaßt, wobei das Verfahren
das Löschen der Zelle durch Anlegen von ungefähr 3 bis 15 Volt an die P+ Source (14), den n-leitenden Quellbereich (18) und den P+ Drain (16) und Anlegen von ungefähr -3 bis -15 Volt an das Kontrollgate (26) umfaßt.

5. Verfahren nach Anspruch 1, wobei die Zelle ferner einen in dem n-leitenden Quellbereich (18) ausgebildeten Auswahltransistor (32) umfaßt, der ein Auswahlgate (36), das an eine Wortleitung angeschlossen ist, eine P+ Source, die an den P+ Drain (16) der Zelle angeschlossen ist, einen P+ Drain (34), der an eine Bitleitung angeschlossen

ist, und einen sich zwischen der P+ Source und dem P+ Drain des Auswahltransistors erstreckenden Channelbereich umfaßt, wobei die Zelle durch eine Versorgungsspannung betrieben und durch Anlegen von ungefähr 5 bis 15 Volt an die P+ Source (14) und den n-leitenden Quellbereich (18), Erden der Wortleitung und der Bitleitung und Anlegen einer von 0 bis auf ungefähr 10 Volt ansteigenden Spannung an das Kontrollgate (26) programmiert wird.

6. Verfahren nach Anspruch 4, wobei die Zelle ferner einen in dem n-leitenden Quellbereich (18) ausgebildeten Auswahltransistor (32) umfaßt, der ein Auswahlgate (36), das an eine Wortleitung angeschlossen ist, eine P+ Source, die an den P+ Drain (16) der Zelle angeschlossen ist, einen P+ Drain (34), der an eine Bitleitung angeschlossen ist, und einen sich zwischen der P+ Source und dem P+ Drain des Auswahltransistors erstreckenden Channelbereich umfaßt, wobei die Zelle durch eine Versorgungsspannung betrieben und durch Anlegen von ungefähr 3 bis 13 Volt an die P+ Source (14), an den n-leitenden Quellbereich (18) und die Bitleitung, Erden der Wortleitung und Anlegen von ungefähr -3 bis -15 Volt an das Kontrollgate (26) gelöscht wird.

7. Verfahren nach Anspruch 1, wobei die Zelle ferner einen Bitleitung-Auswahltransistor (32) umfaßt, der eine P+ Source, die an den P+ Drain (16) der Zelle angeschlossen ist, einen P+ Drain (34), der an eine Bitleitung angeschlossen ist, und ein Auswahlgate (32), das an eine erste Wortleitung angeschlossen ist, hat, sowie einen Source-Auswahltransistor (52) umfaßt, der eine P+ Source (54), einen P+ Drain, der an die P+ Source (14) der Zelle angeschlossen ist, und ein Gate (56), das an eine zweite Wortleitung angeschlossen ist, hat, wobei die Struktur durch eine Versorgungsspannung betrieben und wobei die Zelle durch Anlegen von ungefähr 5 bis 15 Volt an die P+ Source (54) des Source-Auswahltransistors und an den n-leitenden Quellbereich (18), durch Erden der ersten und zweiten Wortleitung und der Bitleitung und durch Anlegen einer von 0 bis auf ungefähr 16 Volt ansteigenden Spannung an das Kontrollgate (26) programmiert wird.

8. Verfahren nach Anspruch 4, wobei die Zelle ferner einen Bitleitung-Auswahltransistor (32) umfaßt, der eine P+ Source, die an den P+ Drain (16) der Zelle angeschlossen ist, einen P+ Drain (34), der an eine Bitleitung angeschlossen ist, und ein Auswahlgate (32), das an eine erste Wortleitung angeschlossen ist, hat, sowie einen Source-Auswahltransistor (52) umfaßt, der eine P+ Source (54), einen P+ Drain, der an die P+ Source (14) der Zelle angeschlossen ist, und ein Gate (56), das an eine zweite Wortleitung angeschlossen ist, hat, wobei die Struktur durch eine Versorgungsspannung betrieben und wobei die Zelle durch Anlegen von ungefähr 3 bis 15 Volt an den n-leitenden Quellbereich (18), die zweite Wortleitung und die Bitleitung, durch Erden der ersten Wortleitung und der P+ Source (54) des Source-Auswahltransistors und durch Anlegen von ungefähr -3 bis -15 Volt an das Kontrollgate (26) gelöscht wird.

Revendications

1. Procédé de commande d'une cellule de mémoire à semiconducteur ayant une région de puits de type N (18) dans laquelle sont formées une source P+ (14), un drain P+ (16) et une région de canal (12) qui s'étend entre la source et le drain, une première couche isolante (24) qui recouvre la région de puits, une grille flottante (22) qui recouvre la première couche isolante, une seconde couche isolante (28) qui recouvre la grille flottante, et une grille de commande (26) qui recouvre la seconde couche isolante, le procédé comprenant :

   la programmation de la cellule par application d'une tension comprise entre environ 5 et 15 V à la source P+ (14) et à la région de puits de type N (18), l'application d'une tension d'environ 0 à 2 V au drain P+ (16), et l'application d'une tension qui varie progressivement d'une tension d'alimentation jusqu'à une valeur aussi élevée que 16 V environ à la grille de commande (26).

2. Procédé de commande d'une cellule de mémoire à semiconducteur ayant une région de puits de type N (18) dans laquelle sont formées une source P+ (14), un drain P+ (16) et une région de canal (12) qui s'étend entre la source et le drain, une première couche isolante (24) qui recouvre la région de puits, une grille flottante (22) qui recouvre la première couche isolante, une seconde couche isolante (28) qui recouvre la grille flottante, et une grille de commande (26) qui recouvre la seconde couche isolante, le procédé comprenant :

   la programmation de la cellule par application d'une tension comprise entre environ 5 et 15 V à la région de puits de type N (18), le couplage de la source P+ (14) à un potentiel flottant, l'application d'une tension d'environ 0 à 2 V au drain P+ (16), et l'application d'une tension comprise entre environ 5 et 16 V à la grille de commande (26).

3. Procédé de commande d'une cellule de mémoire à semiconducteur ayant une région de puits de type N (18) dans laquelle sont formées une source P+ (14), un drain P+ (16) et une région de canal (12) qui s'étend entre la source et le drain, une première couche isolante (24) qui recouvre la région de puits, une grille flottante (22) qui recouvre

la première couche isolante, une seconde couche isolante (28) qui recouvre la grille flottante, et une grille de commande (26) qui recouvre la seconde couche isolante, le procédé comprenant :

l'effacement de la cellule par application d'une tension comprise entre environ 15 et 22 V à la source P+ (14), à la région de puits de type N (18) et au drain P+ (16), et la mise à la masse de la grille de commande (26).

4. Procédé de commande d'une cellule de mémoire à semiconducteur ayant une région de puits de type N (18) dans laquelle sont formées une source P+ (14), un drain P+ (16) et une région de canal (12) qui s'étend entre la source et le drain, une première couche isolante (24) qui recouvre la région de puits, une grille flottante (22) qui recouvre la première couche isolante, une seconde couche isolante (28) qui recouvre la grille flottante, et une grille de commande (26) qui recouvre la seconde couche isolante, le procédé comprenant :

l'effacement de la cellule par application d'une tension comprise entre environ 3 et 15 V à la source P+ (14), à la région de puits de type N (18) et au drain P+ (16), et l'application d'une tension comprise entre environ -3 et -15 V à la grille de commande (26).

5. Procédé selon la revendication 1, dans lequel la cellule comporte en outre un transistor de sélection (32) formé dans la région de puits de type N (18), le transistor de sélection comprenant une grille de sélection (36) couplée à une ligne de mots, une source P+ couplée au drain P+ (16) de la cellule, et un drain P+ (34) couplé à une ligne de bits, et une région de canal qui s'étend entre la source P+ et le drain P+ du transistor de sélection, dans lequel la cellule fonctionne à l'aide d'une tension d'alimentation, et dans lequel la cellule est programmée par application d'une tension comprise entre environ 5 et 15 V à la source P+ (14) et à la région de puits de type N (18), par mise à la masse de la ligne de mots et de la ligne de bits, et par application d'une tension qui varie progressivement de 0 V à 10 V environ à la grille de commande (26).

6. Procédé selon la revendication 4, dans lequel la cellule comporte en outre un transistor de sélection (32) formé dans la région de puits de type N (18), le transistor de sélection comprenant une grille de sélection (36) couplée à une ligne de mots, une source P+ couplée au drain P+ (16) de la cellule, et un drain P+ (34) couplé à une ligne de bits, et une région de canal qui s'étend entre la source P+ et le drain P+ du transistor de sélection, dans lequel la cellule fonctionne à l'aide d'une tension d'alimentation, et dans lequel la cellule est effacée par application d'une tension comprise entre environ 3 et 13 V à la source P+ (14), à la région de puits de type N (18) et à la ligne de bits, par mise à la masse de la ligne de mots, et par application d'une tension comprise entre environ -3 V et -15 V à la grille de commande (26).

7. Procédé selon la revendication 1, dans lequel la cellule comporte en outre un transistor (32) de sélection de ligne de bits ayant une source P+ couplée au drain P+ (16) de la cellule, un drain P+ (34) couplé à une ligne de bits, et une grille de sélection (32) couplée à une première ligne de mots, et un transistor (52) de sélection de source ayant une source P+ (54), un drain P+ couplé à la source P+ (14) de la cellule, et une grille (56) couplée à une seconde ligne de mots, dans lequel la structure travaille à l'aide d'une tension d'alimentation, et dans lequel la cellule est programmée par application d'une tension comprise entre environ 5 et 15 V à la source P+ (54) du transistor de sélection de source et à la région de puits de type N (18), par mise à la masse de la première et de la seconde ligne de mots et de la ligne de bits, et par application d'une tension qui varie progressivement d'une valeur nulle à une valeur aussi élevée que 16 V environ à la grille de commande (26).

8. Procédé selon la revendication 4, dans lequel la cellule comporte en outre un transistor (32) de sélection de ligne de bits ayant une source P+ couplée au drain P+ (16) de la cellule, un drain P+ (34) couplé à une ligne de bits, et une grille de sélection (32) couplée à une première ligne de mots, et un transistor (52) de sélection de source ayant une source P+ (54), un drain P+ couplé à la source P+ (14) de la cellule, et une grille (56) couplée à une seconde ligne de mots, dans lequel la structure fonctionne à l'aide d'une tension d'alimentation, et dans lequel la cellule est effacée par application d'une tension comprise entre environ 3 et 15 V à la région de puits de type N (18), à la seconde ligne de mots, et à la ligne de bits, par mise à la masse de la première ligne de mots et de la source P+ (54) du transistor de sélection de source, et par application d'une tension comprise entre environ -3 et -15 V à la grille de commande (26).

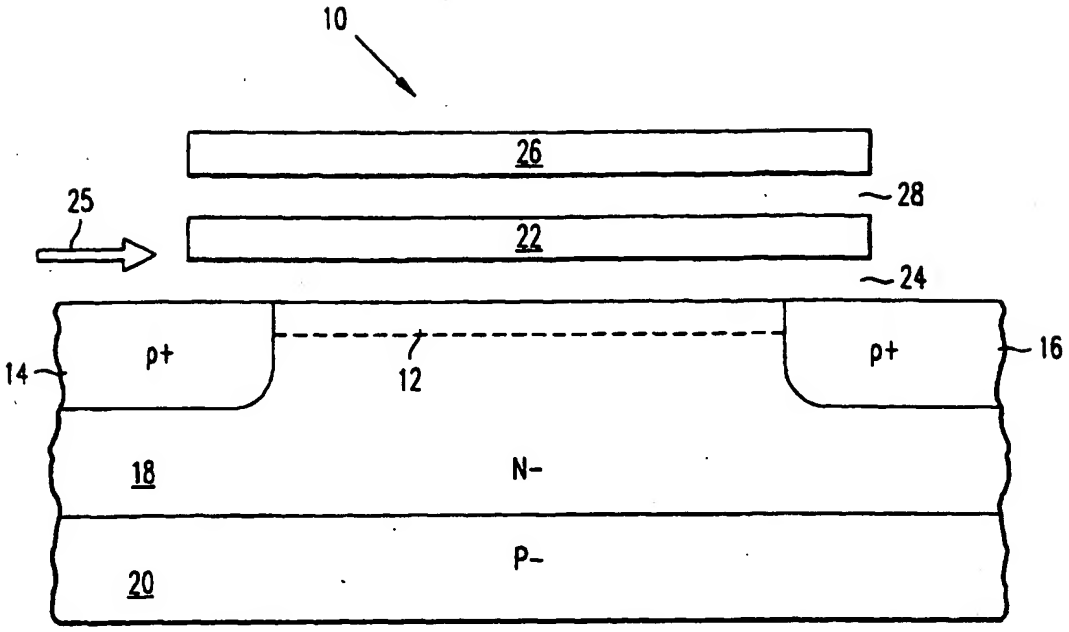
10
26
28
25
22
24
p+
12
p+
16
14
18
N-
P-
20

FIG. 1

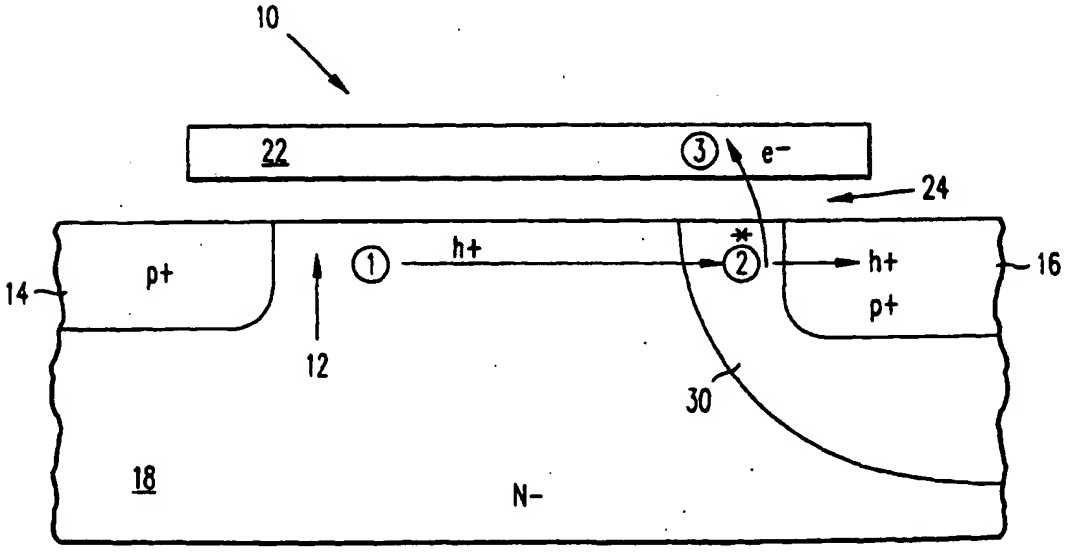
10
22
3
e-
24
p+
1
h+
2
h+
16
14
p+
12
30
18
N-

FIG. 2A

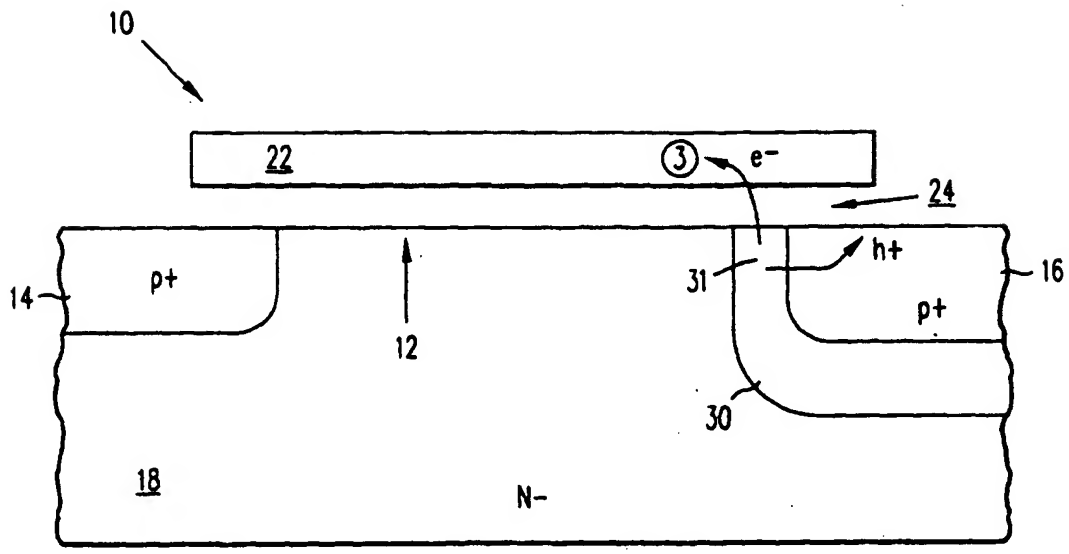

FIG. 2B

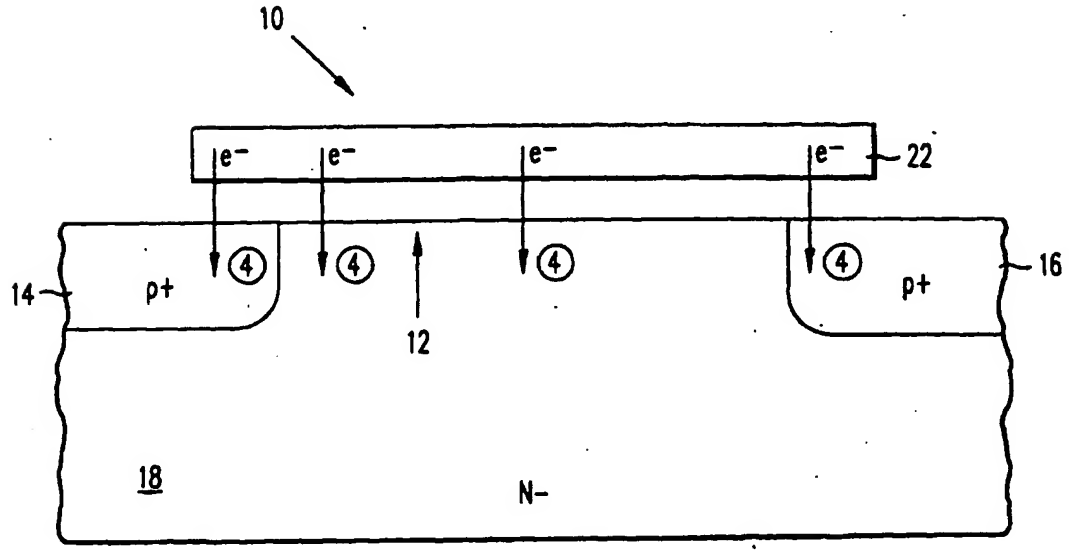

FIG. 2C

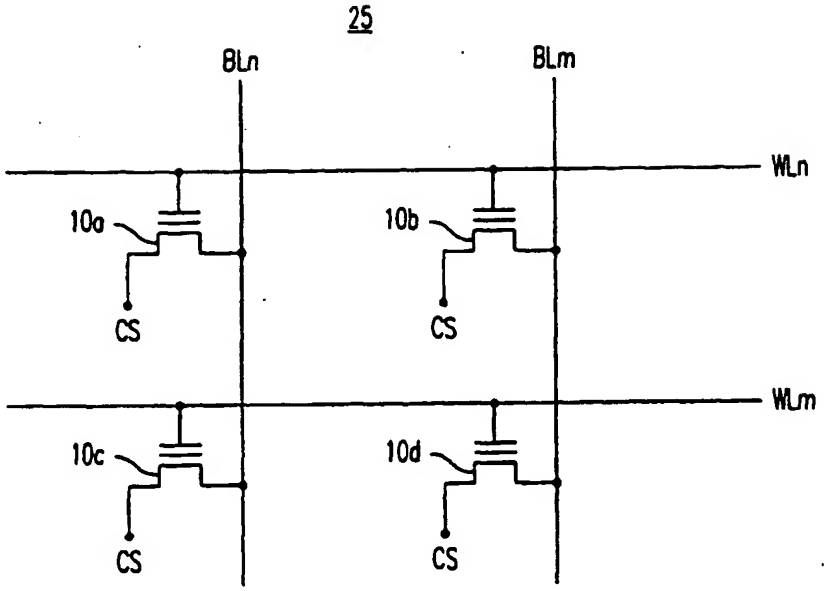
25
BLn
BLm
WLn
10a
10b
CS
CS
WLm
10c
10d
CS
CS

FIG. 3

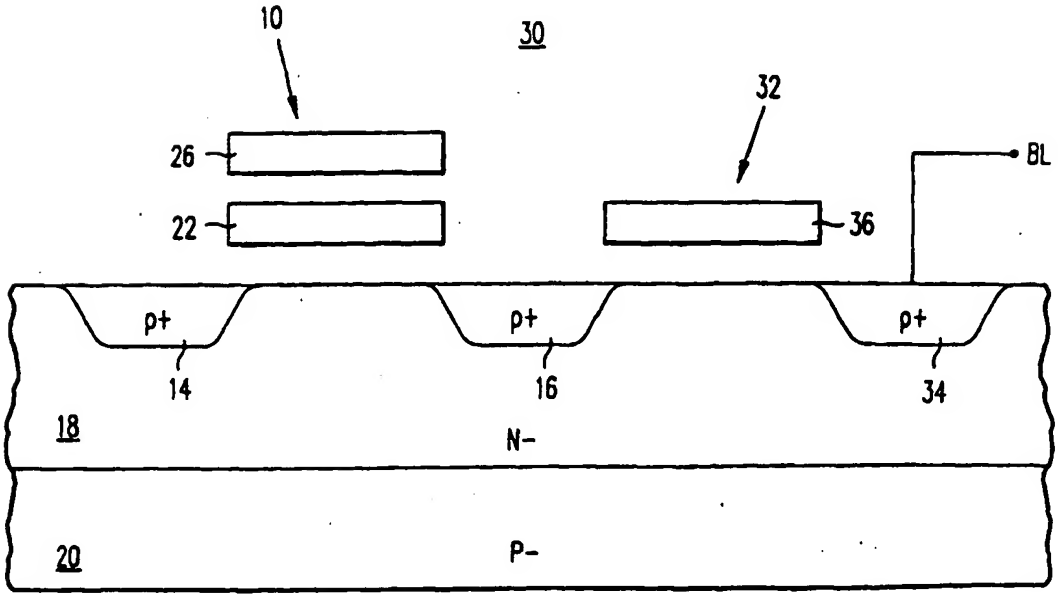
10
30
32
26
22
36
BL
p+
p+
p+
14
16
34
18
N-
20
P-

FIG. 4

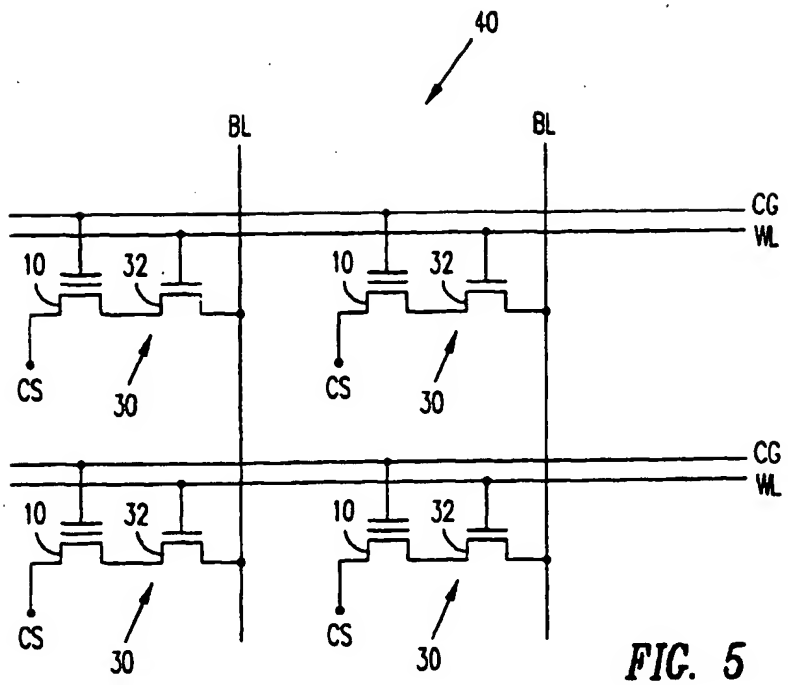
40
BL
BL
CG
WL
10
32
CS
30
CG
WL

FIG. 5

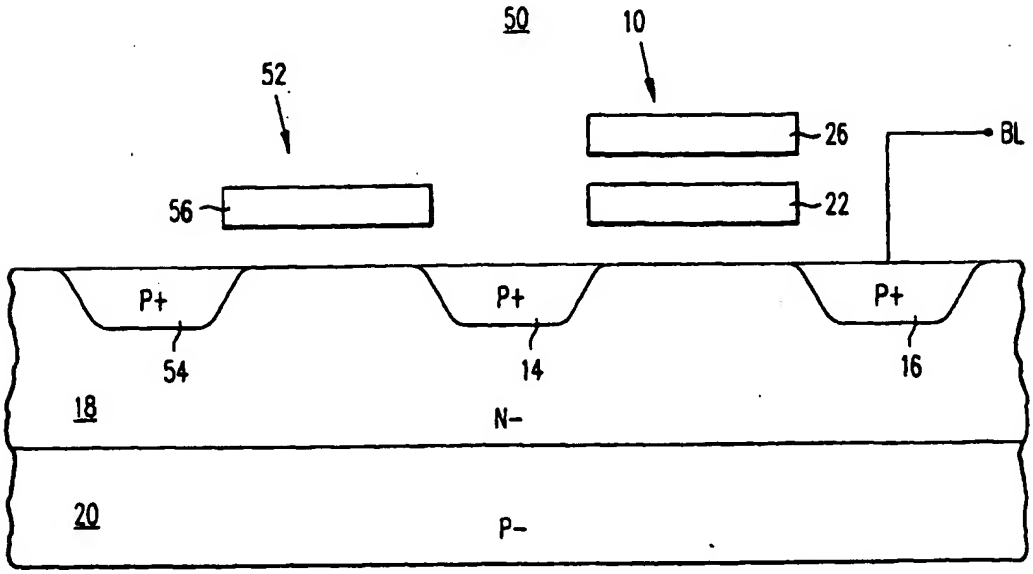
50
10
52
26
BL
56
22
P+
P+
P+
54
14
16
18
N-
20
P-

FIG. 6

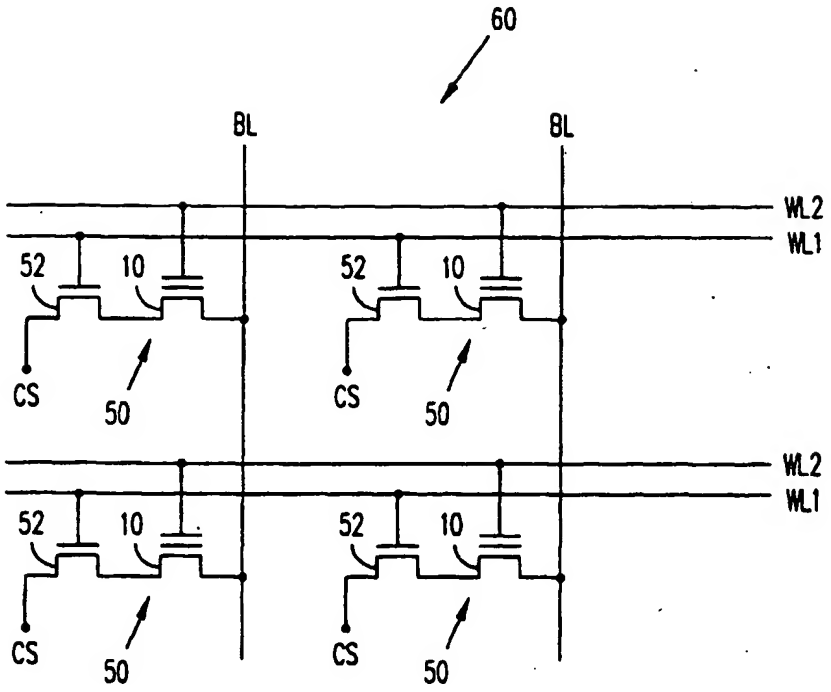
60
BL
BL
WL2
WL1
52
10
CS
50
WL2
WL1

FIG. 7

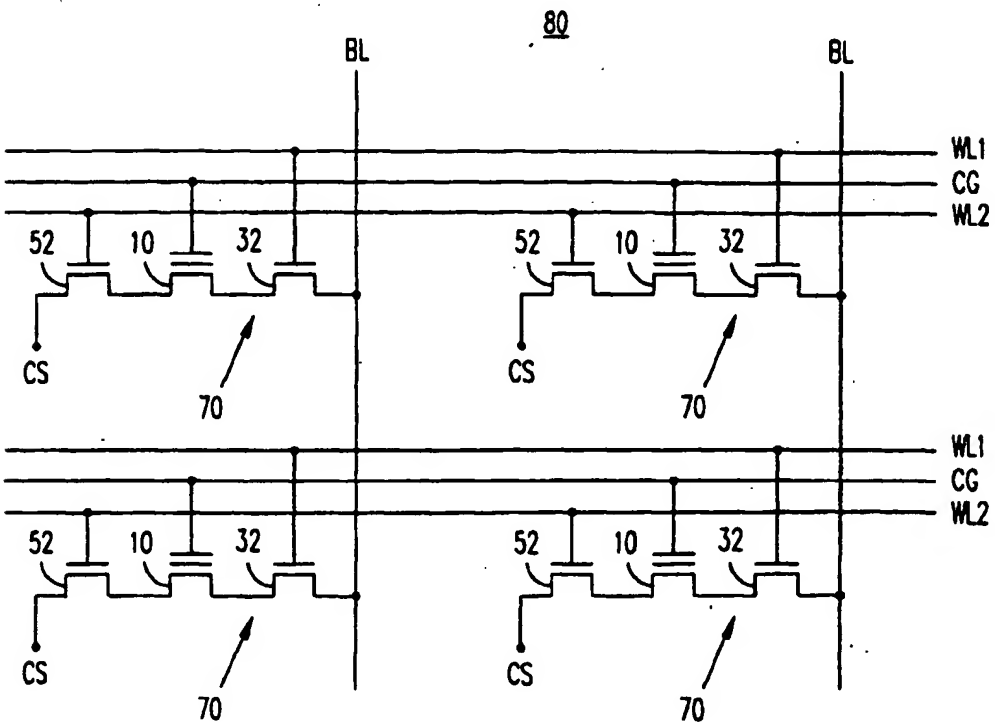
80
BL
BL
WL1
CG
WL2
52
10
32
CS
70

FIG. 9

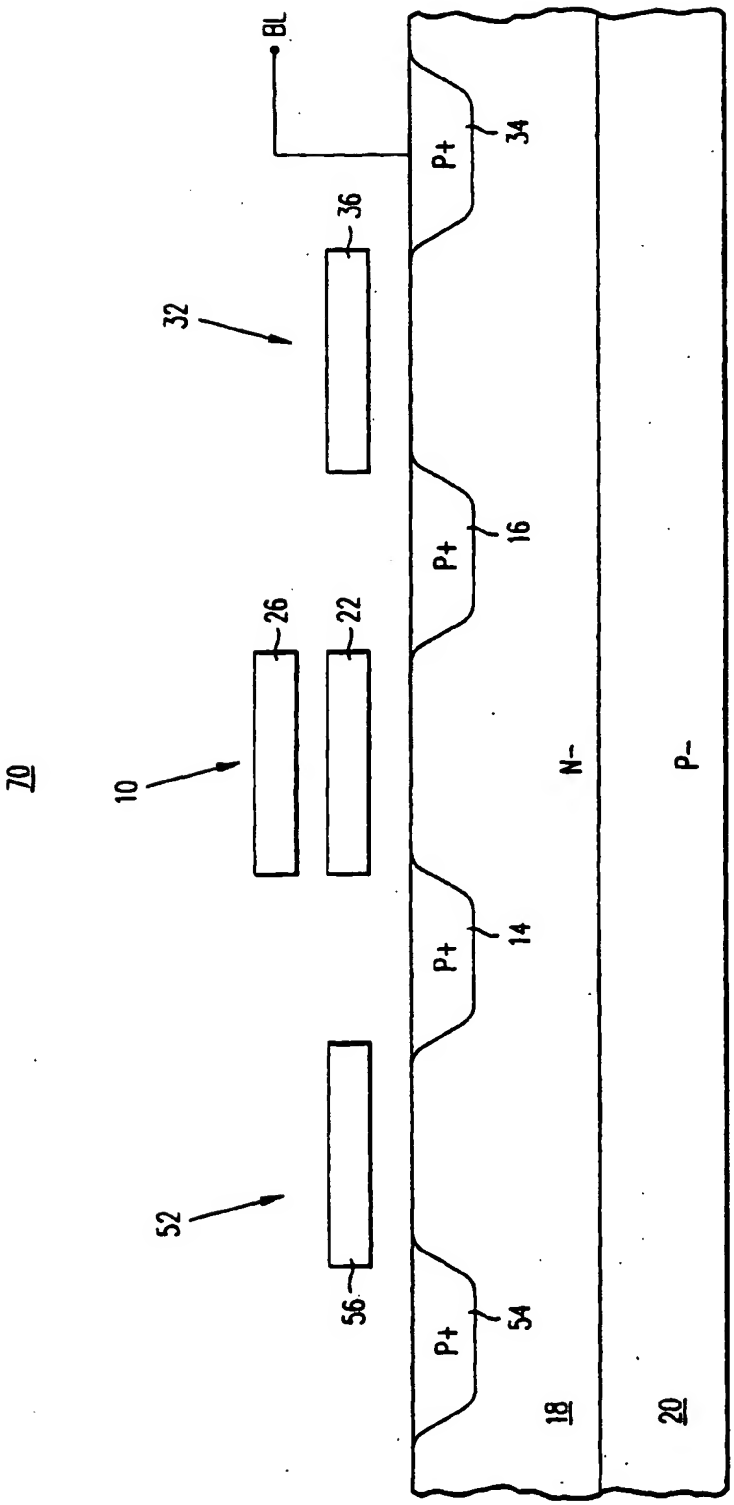

FIG. 8

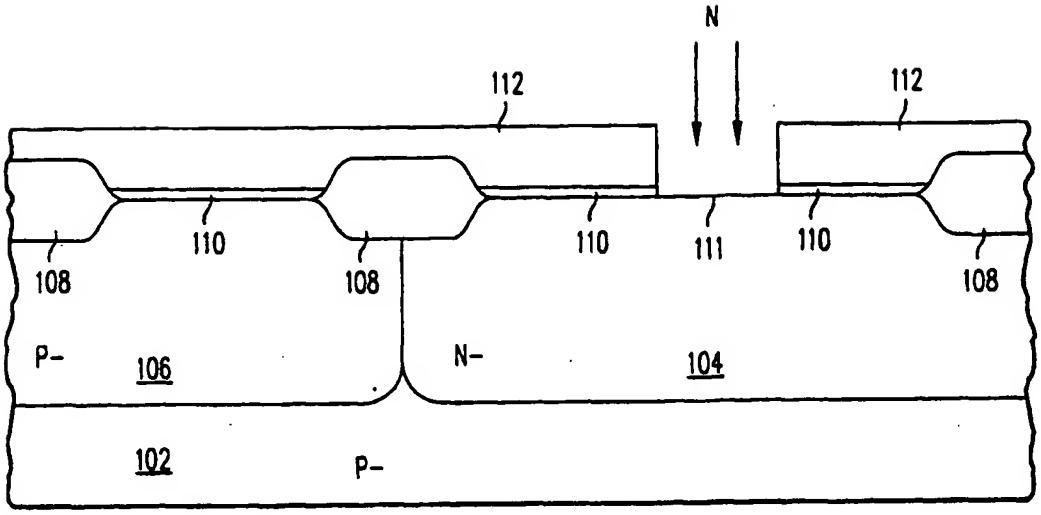
N
112
112
110
110
110
111
108
108
108
P-
106
N-
104
102
P-

FIG. 10

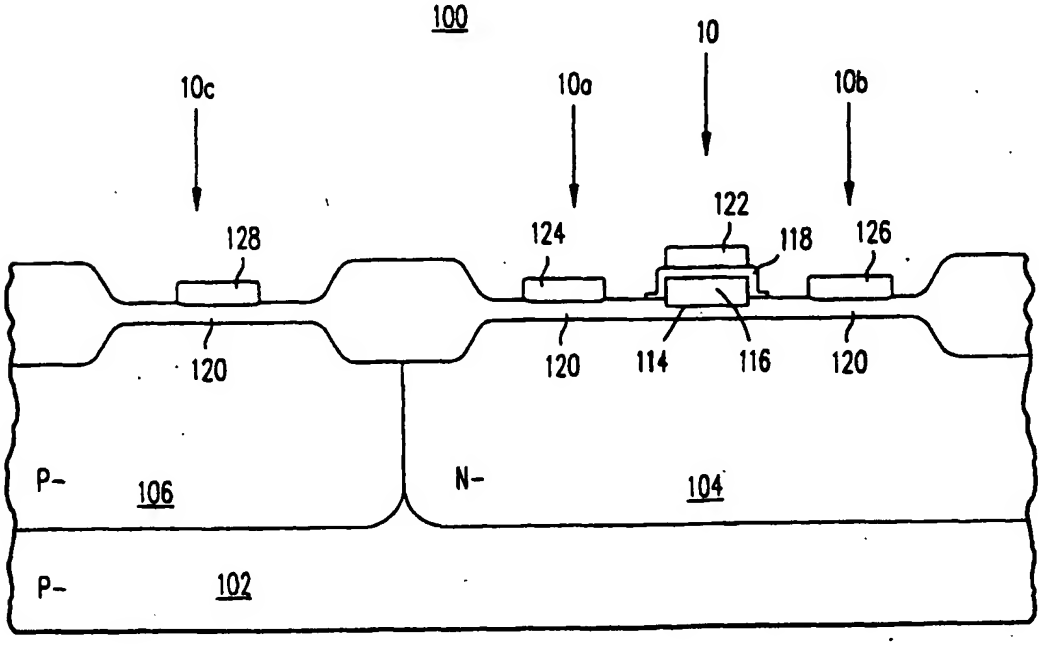
100
10
10c
10a
10b
122
128
124
118
126
120
120
114
116
120
P-
106
N-
104
P-
102

FIG. 11

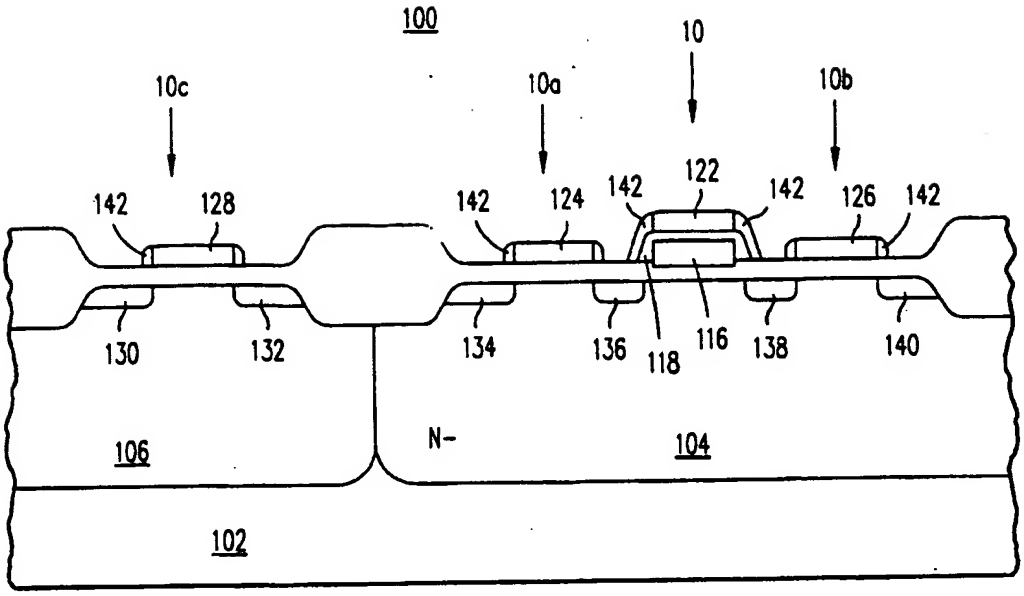
100
10
10c
10a
10b
142
128
142
124
142
122
142
126
142
130
132
134
136
118
116
138
140
106
N-
104
102

FIG. 12

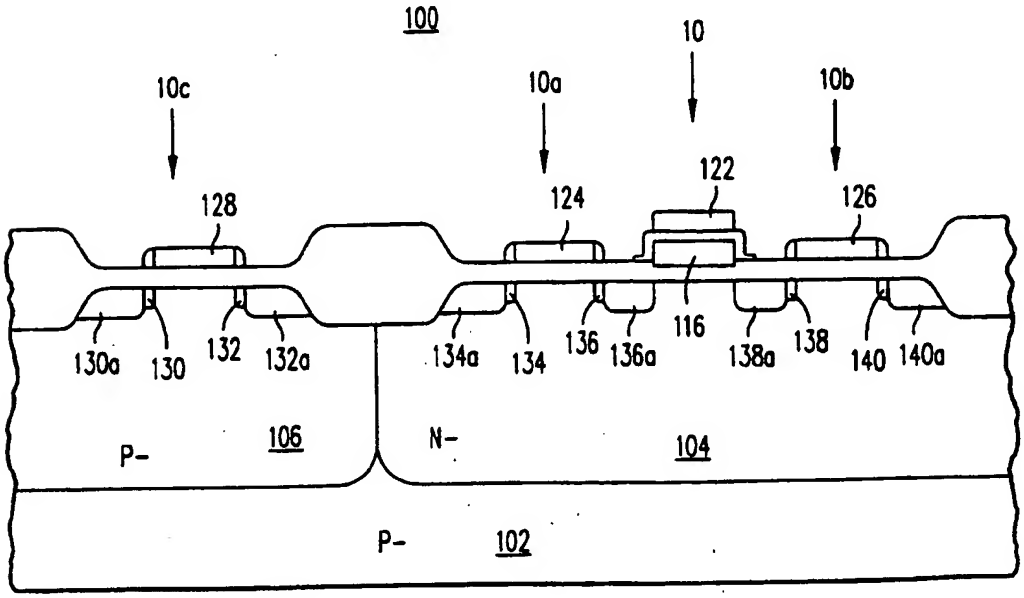
100
10
10c
10a
10b
128
124
122
126
130a
130
132
132a
134a
134
136
136a
116
138a
138
140
140a
P-
106
N-
104
P-
102

FIG. 13